Micro-capacitors based on electrochemically grown vertical arrays of gold nanowires as electrodes

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Abstract

This paper describes the development of micro-capacitors with electrodes based on electrochemically grown vertical gold nanowire arrays. A high aspect-ratio anodized aluminum oxide template integrated on silicon dioxide/silicon substrates was exploited for fabricating a vertical array of nanowires with a high surface to volume ratio. Bismuth ferric oxide thin films were deposited to create high dielectric material between the electrodes using room temperature electrodeposition. This nanofabrication process may be compatible with a complementary metal-oxide-semiconductor (CMOS) process, therefore, this capacitor can be used for protecting and regulating the surge voltage biased to the CMOS circuits. This capacitor achieved a high density capacitance of 3.1 μF/m² at 1 MHz, which was measured using a parallel plate set-up.

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1. Introduction

Integrated circuit (IC) devices are used for most appliances in our daily life. The basic passive elements such as resistors, capacitors, and inductors affect fundamental electrical circuitry characteristics. The parameter value of each component is determined using the requirements of circuitry design. Constant electrical power supply and distribution are critical issues for efficient operations of IC on a chip. System-on-chip devices contain capacitors for regulating and redistributing current flow in the circuit [1,2]. Some erroneous circuit designs and aging effects limit current supply to the IC due to the unstable switching power supply, requiring an additional specific circuit board for supplying and regulating electric power to the main board [3]. This problem can be solved by depositing a capacitance layer on top of circuitry substrate.

Gold (Au) nanowire-based micro-capacitors fabricated onto an IC surface can be used to compensate the power requirement. In this paper, a process which may be complementary metal-oxide-semiconductor (CMOS) compatible for fabricating nanostructured micro-capacitors is presented. This process was developed using Au nanowires on silicon dioxide (SiO₂)/silicon (Si) substrate. Au nanowires were used as the electrode materials for micro-capacitors.

A high aspect-ratio anodized aluminum oxide (AAO) template integrated on SiO₂/Si substrates was used for the fabrication of a vertical array of Au nanowires with high surface-to-volume ratio of about 10⁶:1. The capacitor element was composed of the vertical Au nanowire array embedded in the bismuth ferric oxide (BFO) thin film with a high dielectric constant. The surface area of this capacitor was dramatically increased by adding Au nanowires. This structural combination is expected to enable a high density of capacitance for electrical actuator in micro-circuitry devices due to the increased surface area of this structure.

2. Experimental

2.1. Growth of vertical arrays of gold nanowire on a silicon substrate

Alumina nanoporous templates were formed by oxidizing aluminum film in an anodization process from a previous study [4]. A 50 nm thick titanium (Ti) layer and a 3 μm thick aluminum (Al) layer were deposited on a SiO₂/Si substrate by sputtering. The Si wafer with such thin films of Ti/Al was placed in an electrolytic solution and connected to the positive terminal of a DC power supply as anode, while a counter-electrode (or cathode) was connected to the negative terminal. Under the proper conditions, the anodization of aluminum to produce aluminum oxide caused nanometer sized pores to develop on the film. A two-step anodization process was employed to fabricate ordered arrays of cylindrical nanometer-scale pores on SiO₂/Si substrates. The fabrication of vertical arrays of Au nanowires on the
substrate was performed in the following sequence; (a) first, 50 nm thick titanium (Ti) layer was deposited as an adhesion layer on a SiO2/Si substrate by sputtering; (b) 3 μm thick Al layer was deposited on a SiO2/Si substrate by sputtering; (c) the first anodization (anodic oxidation) of Al layer was carried out to anodize the top 1 μm of Al layer in 0.3 M oxalic acid at a constant voltage of 20 V; (d) the first anodized Al layer was selectively removed by immersion in 4 vol.% CrO3 + 6 vol.% H3PO4 solution for 18 h at room temperature; (e) the second anodization was conducted under the same conditions as the first step and lasted until the Al film was completely converted to alumina; (f) cathodic electrodeposition was performed to grow about 2 μm long Au nanowires in the pores of templates on a SiO2/Si substrate. Au nanowires were galvanostatically electrodeposited in an Au bath prepared with 0.4 mol/L (100 g/L) of tri ammonium citrate, 0.07 mol/L (25 g/L) of KAuCl4 and 0.54 mol/L (68.5 g/L) of Na2SO3 in 500 ml of deionized (DI) water solution at a constant current density of 5 mA/cm2 using potentiostat/galvanostat model VMC-4 of Princeton Applied Research; (g) finally, the wet etching to remove the AAO template layer with 0.1 M NaOH was carried out to expose the Au nanowires on a SiO2/Si substrate. A schematic cross-sectional view of the device is shown in Fig. 1.

2.2. Electrodeposition of BFO thin film

BFO thin films exhibit high dielectric constant (about 1000 at 100 Hz) and thus are attractive as dielectric materials for capacitor applications [5]. BFO thin films were coated on the surface and top of the vertical array of Au nanowires by electrodeposition at room temperature using an aqueous metal nitrate bath, which was prepared by a mixture of 0.1 M Bi(NO3)3 and 0.1 M Fe(NO3)3. The electrodeposition was carried out under galvanostatic mode at 6 mA/cm2 for 30 min. A niobium (Nb) electrode was used as a reference electrode for BFO electrodeposition. Fig. 2 shows the chronopotentiogram for the deposition of the BFO films at constant current (6 mA/cm2). The cathodic potential decreased gradually and stabilized at about −1.4 V. Typically, the potential during the deposition process was between −1.4 V and 1.5 V.

3. Results and discussion

3.1. Material characterization

Fig. 3 shows a field emission scanning electron microscope (FESEM) cross-sectional view of Au nanowires embedded in BFO dielectric films. The Au nanowires were well aligned vertically with an average diameter of about 50–60 nm. The length of nanowires was about 2 μm. In the FESEM image the Au nanowires are brighter than BFO because atomic number of Au is higher than average atomic number of BFO. The composition of the resulting Au nanowire-embedded in BFO films was determined with X-ray energy dispersive

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Fig. 1. (A) Top-view of the micro-capacitor and (B) schematic cross-sectional view of the micro-capacitor. A gold film of 10 mm × 10 mm sputtered on the top surface of the capacitor. The micro-capacitor consists of a vertical array of Au nanowires embedded in BFO film on a silicon substrate.

Fig. 2. Chronopotentiogram of the deposition of BFO films on Au nanowires. The cathodic potential decreases gradually and stabilized at about −1.4 V indicating stable deposition of BFO films.

Fig. 3. (A) FESEM images of cross-sectional view of Au nanowires embedded in BFO films on a silicon substrate at low magnification and (B) FESEM image of cross-sectional view of Au nanowires embedded in BFO films on a Si at high magnification. The arrows (a) and (b) indicate ‘Au nanowires’ and ‘BFO films’, respectively. The Au nanowires were well aligned vertically with an average diameter of about 50–60 nm.
spectroscopy (EDS). Fig. 4 shows the EDS data obtained from a cross-section of the device. The characteristic results using EDS confirmed the fabrication of Au nanowires on the BFO film.

3.2. Electrical characterization

3.2.1. Measurement

The capacitance of the micro-capacitor was measured with a LCR meter (HP-4284A, Hewlett-Packard) using a two-probe method in the frequency range 100 Hz to 1 MHz. A gold film of 10 mm × 10 mm sputtered on the top surface of the capacitor and a Ti layer on the bottom surface were used as electrodes for the measurement of the capacitance.

3.2.2. Capacitance and effective dielectric constant

The parallel plate capacitance \( C_p \) was measured with respect to frequency \( f \) and applied voltage at room temperature, and then used to calculate the dielectric constant \( \varepsilon_r \).

\[
\varepsilon_{r,\text{eff}} = \frac{C_p \times t_a}{A \times \varepsilon_0} \tag{1}
\]

where, \( C_p \) (unit: Farad) is the capacitance of the micro-capacitor, \( t_a \) (unit: mm) is the apparent thickness of the capacitor, the distance between top and bottom electrode surfaces, \( A \) (unit: \( m^2 \)) is the area of upper electrode surface and \( \varepsilon_0 \) is the dielectric constant of free space \((8.85 \times 10^{-12} \text{ F/m})\). The capacitance of 3.1 \( \mu \text{F/m}^2 \) at 1 MHz was achieved. The capacitance density was calculated by the measured value of capacitance divided by the surface area.

Fig. 5 shows the capacitance and the effective dielectric constant of the capacitor, respectively. Both values decreased drastically in the 100 Hz to 10 kHz frequency range, and then were kept almost constant up to 1 MHz. This is consistent with the intrinsic characteristic of the dielectric constant of BFO thin films [6], which is attributed to spontaneous polarization of the perovskite structure of ferroelectric ceramics. The measured dielectric constant was higher than that of bulk BFO (about 290 at 100 Hz) [7].

4. Conclusions

The micro-capacitor was fabricated using Au nanowires on a silicon substrate. A vertical array of Au nanowires was grown on a silicon substrate by electrodeposition using an AAO nanoporous template. Subsequently, electrodeposition of BFO resulted in Au nanowires embedded in BFO films. The high density capacitance of 3.1 \( \mu \text{F/m}^2 \) at 1 MHz was achieved.

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